National Semiconductor

MICROCIRCUIT DATA SHEET

MNCLC410A-X REV 0A0

Original Creation Date: 11/03/98
Last Update Date: 07/19/99
Last Major Revision Date: 05/06/99

FAST SETTLING, VIDEO OP AMP WITH DISABLE

General Description

The current-feedback CLC410 is a fast-settling, wideband, monolithic op amp with fast disable/enable feature. Designed for low-gain applications (Av = ±1 to ±8), the CLC410 consumes only 160mW of power (180mW max) yet provides a -3dB bandwidth of 200MHz (Av = +2) and 0.05% settling in 12ns (15ns max). Plus, the disable feature provides fast turn-on (100ns) and turn-off (200ns). In addition, the CLC410 offers both high performance and stability without compensation, even at a gain of +1.

The CLC410 provides a simple, high-performance solution for video switching and distribution applications, especially where analog buses benefit from use of the disable function to "multiplex" signals onto the bus. Differential gain/phase of 0.01%/0.01 provide high fidelity and the 70mA output current offers ample drive capability.

The CLC410's fast settling, low distortion, and high drive capabilities make it an ideal ADC driver. The low 160mW quiescent power consumption and very low 40mW disabled power consumption suggest use where power is critical and/or "system off" power consumption must be minimized.

Industry Part Number

CLC410A

NS Part Numbers

CLC410AJ-QML

Prime Die

UB1286C

Controlling Document

5962-9060001PA

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- -3dB bandwidth of 200MHz
- 0.05% settling in 12ns
- Low power, 160mW (40mW disabled)
- Low distortion, -60dBc at 20MHz
- Fast disable (200ns)
- Differential gain/phase: 0.01%/0.01 deg
- ±1 to ±8 closed-loop gain range

Applications

- Video switching and distribution
- Analog bus driving (with disable)
- Low power "standby" using disable
- Fast, precision A/D conversion
- D/A current-to-voltage conversion
- IF processors
- High-speed communications

(Absolute Maximum Ratings)

(Note 1)

Supply Voltage (Vs)	±7V dc
Output Current (Iout)	70mA
Common Mode Input Voltage (Vcm)	±Vs
Differential Input Voltage (Vid)	5V
Disable Input Voltage (D I S pin)	+Vs
Applied Output Voltage when Disabled	±Vs
Maximum Power Dissipation (Pd) (Note 2)	1.2W
Lead Temperature (soldering, 10 seconds)	+300 C
Junction Temperature (Tj)	+175 C
Storage Temperature	-65 C to +150 C
Thermal Resistance	
Junction -to-ambient (ThetaJA)	
Ceramic DIP (Still Air) (500 LFPM)	TBD
Junction -to-case (ThetaJC)	
Ceramic DIP	TBD
Package Weight (Typical)	
Ceramic DIP	TBD
ESD Tolerance (Note 3)	
ESD Rating	1000V

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA) / ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Human body model, 100pF discharged through 1.5K Ohms.

Recommended Operating Conditions

Supply Voltage (Vs)	±5V dc
Gain Range (Av)	±1 to ±8
Ambient Operating Temperature Range (Ta)	-55 C to +125 C

Electrical Characteristics

AC/DC PARAMETERS: ELECTRICAL CHARACTERISTICS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vs = ±5V dc, Av = +2, load resistance (Rl = 100Ohms), feedback resistance (Rf) = 250Ohms, gain setting resistance (Rg) = 250Ohms. -55 C ≤ Ta ≤ +125 C (Note 3).

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
+Iin	Input Bias Current (noninverting)				-20	+20	uA	1, 2
					-36	+36	uA	3
-Iin	Input Bias Current (Inverting)				-20	+20	uA	1
					-30	+30	uA	2
					-36	+36	uA	3
Vio	Input Offset Voltage	Rs = 50 Ohms			-5.0	+5.0	mV	1
					-9.0	+9.0	mV	2
					-8.2	+8.2	mV	3
Tc (+Iin)	Average +Input Bias Current Drift		1		-100	+100	nA/C	2
			1		-200	+200	nA/C	3
Tc (-Iin)	Average -Input Bias Current Drift		1		-100	+100	nA/C	2
			1		-200	+200	nA/C	3
Tc (Vio)	Average Offset Voltage Drift		1		-40	+40	uV/C	2, 3
Is	Supply Current	No Load				18	mA	1, 2, 3
PSRR	Power Supply Rejection Ratio	Vs+ = +4.5V to +5.0V, Vs- = -4.5V to -5.0V			45		dB	1, 2, 3
CMRR	Common Mode Rejection Ratio	Vcm = ±1 V	1		45		dB	1, 2, 3
SSBW	Small Signal Bandwidth	-3 dB bandwidth, Vout < 0.5 Vpp			150		MHz	4
			2		120		MHz	5
			2		150		MHz	6
GFPL	Gain Flatness Peaking Low	At 0.1 Mhz to 40 MHz				0.3	dB	4
			2			0.4	dB	5, 6
GFPH	Gain Flatness Peaking High	At > 40 MHz				0.5	dB	4
			2			0.7	dB	5, 6
GFR	Gain Flatness Rolloff	At 0.1 Mhz to 75 MHz				1	dB	4
			2			1.3	dB	5
			2			1	dB	6

Electrical Characteristics

AC/DC PARAMETERS: ELECTRICAL CHARACTERISTICS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vs = ±5V dc, Av = +2, load resistance (Rl = 100Ohms), feedback resistance (Rf) = 250Ohms, gain setting resistance (Rg) = 250Ohms. -55 C ≤ Ta ≤ +125 C (Note 3).

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
HD2	Second Harmonic Distortion	2 Vpp at 20 MHz				-45	dBc	4
			2			-45	dBc	5
			2			-40	dBc	6
HD3	Third Harmonic Distortion	2 Vpp at 20 MHz				-50	dBc	4
			2			-50	dBc	5, 6
SNF	Noise Floor	At > 1 MHz	1			-154	dBm (1Hz)	4, 6
			1			-156	dBm (1Hz)	5
INV	Integrated Noise	At 1 MHz to 200 Mhz	1			57	uV	1
			1			63	uV	2
			1			54	uV	3
Vdis	DISABLE voltage to disable		1			0.5	V	1, 2, 3
Ven	DISABLE voltage to enable		1			3.2	V	1
			1			4.0	V	2
			1			2.3	V	3
Idis	DISABLE current to disable		1			250	uA	1, 2, 3
Ien	DISABLE current to enable		1			60	uA	1, 2, 3
OSD	Off Isolation	At 10 Mhz	1			55	dB	4, 5, 6
Toff	Disable Time	> 50 dB attenuation at 10 Mhz	1			1000	ns	4, 5, 6
Ton	Enable Time		1			200	ns	4, 5, 6
TRS	Rise and Fall Time	0.5 V Step	1			2.4	ns	9, 10, 11
TRL	Rise and Fall Time	5 V Step	1			10	ns	9, 10, 11
+Rin	Input Resistance		1		100		kOhm	1, 2
			1		50		kOhm	3
Iout	Output Current		1		50		mA	1, 2
			1		30		mA	3

Electrical Characteristics

AC/DC PARAMETERS: ELECTRICAL CHARACTERISTICS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vs = ±5V dc, Av = +2, load resistance (Rl = 100Ohms), feedback resistance (Rf) = 250Ohms, gain setting resistance (Rg) = 250Ohms. -55 C ≤ Ta ≤ +125 C (Note 3).

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vout	Output Voltage Swing	Rl = 100 Ohms	2		2.8		V	4, 5
			2		2.3		V	6
SR	Slew Rate	Measured ±1 V with ±3 V step, Av = +2	1		430		V/uS	4, 5, 6
ts	Settling Time	2 V step at 0.1% of the fixed value	1			13	ns	9, 10, 11
		2 V step at 0.05% of the fixed value	1			15	ns	9, 10, 11
OS	Overshoot	0.5 V step	1			10	%	9, 10
			1			15	%	11

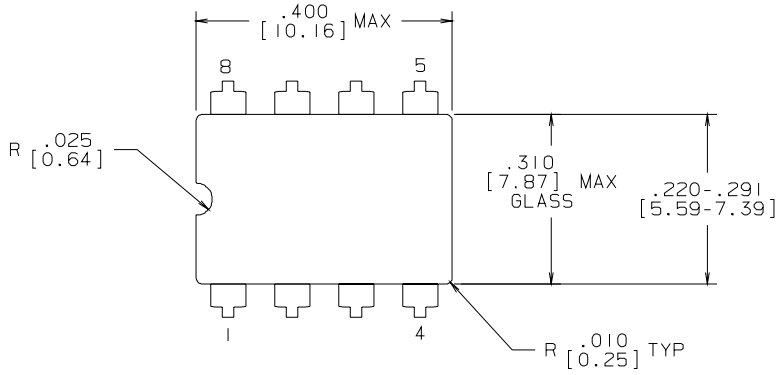
Note 1: If not tested, shall be guaranteed to the limits specified in table 1 herein.
Note 2: Group A sample tested only.
Note 3: The algebraic convention, whereby the most negative value is a minimum and most positive is a maximum, is used in this table. Negative current shall be defined as convential current flow out of a device terminal.

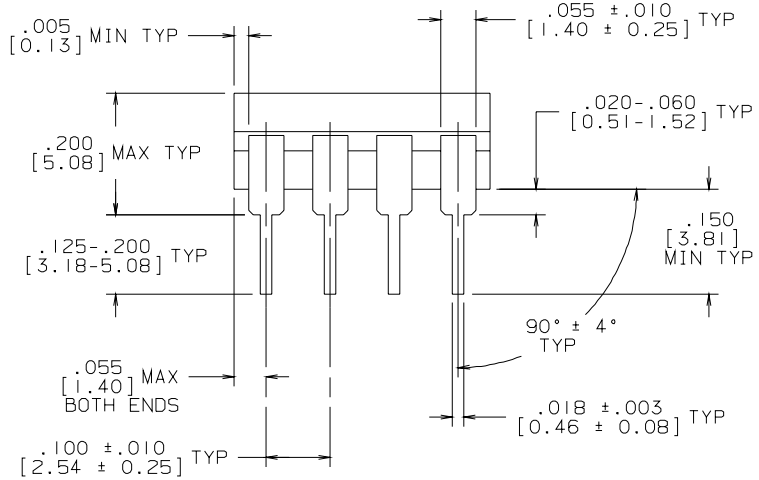
Graphics and Diagrams

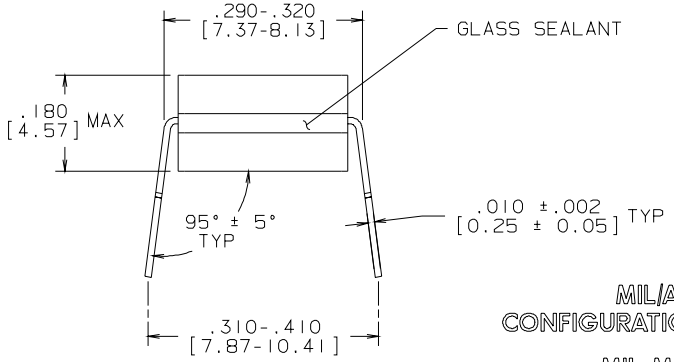
GRAPHICS#	DESCRIPTION
07081HRA3	CERDIP (J), 8 LEAD (B/I CKT)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000416A	CERDIP (J), 8 LEAD (PINOUT)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/







MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

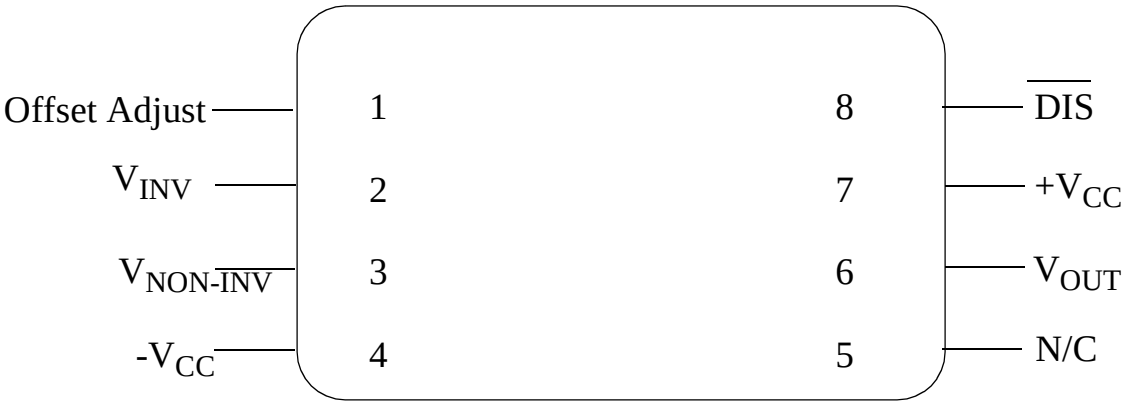
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 8 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1



CLC410J

8 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

P000416A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003072	07/19/99	Shaw Mead	Initial MDS Release